Amendments to the Claims

This listing of the Claims will replace all prior versions and listings of the claims in this patent application.

Listing of the Claims

Claims 1-105 (canceled)

106. (previously presented) A semiconductor chip connected to a wirebond interconnect, comprising:

a silicon substrate;

a transistor in or on said silicon substrate;

a metallization structure over said silicon substrate, wherein said metallization structure comprises a first metal layer and a second metal layer over said first metal layer;

a dielectric layer between said first and second metal layers;

a first contact pad over said silicon substrate, wherein said first contact pad has a top surface with a first region and a second region, wherein said second region surrounds said first region;

a passivation layer over said metallization structure, over said dielectric layer and on said second region, wherein said passivation layer has a thickness greater than that of said dielectric layer, wherein a first opening in said passivation layer is over said first region and exposes said first region, wherein said first opening has a size between 0.1 and 50

micrometers, and wherein said passivation layer comprises an oxide layer and a nitride layer over said oxide layer;

a polymer layer on said passivation layer, wherein a second opening in said polymer layer is over said first region and exposes said first region, and wherein said polymer layer has a thickness between 2 and 50 μm, greater than that of said dielectric layer and greater than that of said passivation layer;

a second contact pad connected to said wirebond interconnect, wherein said second contact pad comprises an electroplated gold layer with a thickness between 2 and 100 μm, wherein said second contact pad is connected to said first contact pad through said first and second openings, and wherein the positions of said first and second contact pads from a top perspective view are different; and

a signal interconnect on said polymer layer, wherein said second contact pad is connected to said first contact pad through said signal interconnect.

Claims 107-109 (canceled)

110. (previously presented) The semiconductor chip of claim 106, wherein said second contact pad further comprises a titanium-containing layer under said electroplated gold layer.

Claim 111 (canceled)

112. (currently amended) The semiconductor chip of claim 110, wherein said titanium-containing layer comprises tungsten.~~.~~

113. (previously presented) The semiconductor chip of claim 110, wherein said titanium-containing layer comprises nitrogen.

114. (previously presented) The semiconductor chip of claim 106, wherein said polymer layer comprises polyimide.

Claims 115-119 (canceled)

120. (previously presented) A semiconductor chip connected to a wirebond interconnect, comprising:

a silicon substrate;

a transistor in or on said silicon substrate;

a metallization structure over said silicon substrate, wherein said metallization structure comprises a first metal layer and a second metal layer over said first metal layer;

a dielectric layer between said first and second metal layers;

a first contact pad over said silicon substrate;

a passivation layer over said metallization structure and over said dielectric layer, wherein said passivation layer has a thickness greater than that of said dielectric layer, and wherein said passivation layer comprises an oxide layer and a nitride layer over said oxide layer;

a polymer layer on said passivation layer, wherein an opening in said polymer layer is over said first contact pad and exposes said first contact pad, and wherein said polymer layer

has a thickness between 2 and 50 μm, greater than that of said dielectric layer and greater than that of said passivation layer;

a second contact pad connected to said wirebond interconnect, wherein said second contact pad comprises an electroplated gold layer with a thickness between 2 and 100 μm, wherein said second contact pad is connected to said first contact pad through said opening, and wherein the positions of said first and second contact pads from a top perspective view are different; and

a signal interconnect on said polymer layer, wherein said second contact pad is connected to said first contact pad through said signal interconnect.

Claims 121-135 (canceled)

136. (previously presented) A semiconductor chip connected to a wirebond interconnect, comprising:

a silicon substrate;

a transistor in or on said silicon substrate;

a metallization structure over said semiconductor substrate, wherein said metallization structure comprises a first metal layer and a second metal layer over said first metal layer;

a dielectric layer between said first and second metal layers;

a first contact pad over said silicon substrate, wherein said first contact pad has a top surface with a first region and a second region, wherein said second region surrounds said first region;

a passivation layer over said metallization structure, over said dielectric layer and on said second region, wherein said passivation layer has a thickness greater than that of said dielectric layer, wherein a first opening in said passivation layer is over said first region and exposes said first region, wherein said first opening has a size between 0.1 and 50 micrometers, and wherein said passivation layer comprises an oxide layer and a nitride layer over said oxide layer;

a polymer layer on said passivation layer, wherein a second opening in said polymer layer is over said first region and exposes said first region, and wherein said polymer layer has a thickness between 2 and 50 μm, greater than that of said dielectric layer and greater than that of said passivation layer;

a second contact pad connected to said wirebond interconnect, wherein said second contact pad comprises a titanium-containing layer with a thickness between 0.01 and 3 μm, a seed layer with a thickness between 0.05 and 3 μm over said titanium-containing layer, and an electroplated gold layer with a thickness between 2 and 100 μm on said seed layer, wherein said second contact pad is connected to said first contact pad through said first and second openings, and wherein the positions of said first and second contact pads from a top perspective view are different; and

a signal interconnect on said polymer layer, wherein said second contact pad is connected to said first contact pad through said signal interconnect.

Claims 137-140 (canceled)

141. (previously presented) The semiconductor chip of claim 110, wherein said titanium-containing layer has a thickness between 0.01 and 3 μm.

142. (previously presented) The semiconductor chip of claim 110, wherein said second contact pad further comprises a seed layer between said titanium-containing layer and said electroplated gold layer, wherein said seed layer has a thickness between 0.05 and 3 μm.

143. (previously presented) The semiconductor chip of claim 120, wherein said second contact pad further comprises a titanium-containing layer under said electroplated gold layer.

144. (previously presented) The semiconductor chip of claim 143, wherein said titanium-containing layer has a thickness between 0.01 and 3 μm.

145. (previously presented) The semiconductor chip of claim 143, wherein said second contact pad further comprises a seed layer between said titanium-containing layer and said electroplated gold layer, wherein said seed layer has a thickness between 0.05 and 3 μm.

Claims 146-152 (canceled)

153. (previously presented) The semiconductor chip of claim 136, wherein said polymer layer comprises polyimide.

Claim 154 (canceled)

155. (previously presented) The semiconductor chip of claim 120, wherein said polymer layer comprises polyimide.